REMARKS

In an Office Action mailed on November 26, 2004, claims 1, 2, 16 and 17 were rejected under 35 U.S.C. § 102(e) as being anticipated by O'Connor; claims 3-6, 8-14, 18-21 and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over O'Connor in view of Silvestri; and claims 7, 15 and 22 were objected to as being dependent upon rejected base claims but were indicated as being allowable if rewritten in independent form. Newly-added claims 24-28 are patentable in view of the cited art for at least the reason that none of the cited art teaches or suggests instructions to, when executed by a processor-based system, cause the processor-based system to control a locked loop circuit. The §§ 102 and 103 rejections are discussed below.

§ 102 Rejections:

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by O'Connor. The system of claim 1 includes a locked loop circuit and a processor. The processor is coupled to the locked loop circuit to control the locked loop circuit and perform at least one other function in the system not related to the control of the locked loop circuit.

Contrary to the limitations of independent claim 1, O'Connor discloses processors 210, 212 and 218; and O'Connor also discloses memory data controllers, such as the memory data controllers 260, 262 and 264 that are depicted in Fig. 3. O'Connor also recites that the clock generation circuitry may be one or more phase locked loop (PLL) or delay locked loop (DLL) circuits. O'Connor, 3:12-19. O'Connor also discloses that clock signals that have been routed through a portion of a memory array 270 are sent back to the memory data controllers as feedback signals. *See, for example,* O'Connor, 3:43-53.

However, there is no teaching or even a suggestion in O'Connor regarding control of any of the DLL or PLL circuits by a processor, such as the processors 210, 212 or 218. Therefore, for at least this reason, O'Connor fails to anticipate independent claim 1.

Independent claim 16 also stands rejected under 35 U.S.C. § 102(e) as being anticipated by O'Connor. The method of claim 16 includes providing a locked loop circuit that has a processor accessible interface. The method includes using a processor to control the locked loop circuit and perform at least one other function not related to the control of the locked loop circuit.

See discussion of independent claim 1 above. In particular, there is no teaching or even a suggestion in O'Connor regarding a locked loop circuit that has a processor accessible interface

so that a processor may be used to control the locked loop circuit. Thus, for at least this reason, O'Connor fails to anticipate independent claim 16.

Claims 2 and 17 overcome the § 102(e) rejections for at least the reason that these claims depend from allowable independent claims. Therefore, for at least the reasons that are set forth above, withdrawal of the § 102(e) rejections of claims 1, 2, 16 and 17 is requested.

§ 103(a) Rejections:

The § 103(a) rejections are based on the combination of O'Connor in view of Silvestri. However, the § 103(a) rejections are overcome for at least the reason that O'Connor may not be used as a § 103 reference against any of the claims in the present application. More specifically, O'Connor qualifies as prior art only under 35 U.S.C. § 102(e). The subject matter that is set forth in O'Connor and the invention that is set forth in the claims were commonly owned at the time the invention was made by Intel Corporation, the assignee of the present application, as shown in the recorded assignment attached as Exhibit A. Thus, pursuant to 35 U.S.C. § 103(c), O'Connor cannot be used as a § 103 rejection against the claims of the present application. M.P.E.P. § 2146. Therefore, for at least this reason, withdrawal of all of the § 103(a) rejections is requested.

CONCLUSION

In view of the foregoing, withdrawal of the §§ 102 and 103 rejections and a favorable action in the form of a Notice of Allowance are requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504 (ITL.0550US).

Respectfully submitted,

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